Electrical properties of $LaAlO_3/Si$ and $Sr_{0.8}Bi_{2.2}Ta_2O_9/LaAlO_3/Si$ structures

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Lanthanum aluminate ($LaAlO_3$) films were deposited on Si(100) substrates by evaporating single-crystal pellets in vacuum using an electron-beam gun. Then, they were annealed in N_2 ambience at 700 °C for 10 min using an electric furnace. X-ray diffraction analysis showed that the $LaAlO_3$ films were amorphous even after the annealing process. No hysteretic characteristics were observed in the capacitance–voltage ($C-V$) measurement and the dielectric constant of the $LaAlO_3$ films was estimated to be 21–25. It was also found that the leakage current density decreased by about three orders of magnitude after the annealing process. On these films, $Sr_{0.8}Bi_{2.2}Ta_2O_9$ films with 210 nm thickness were deposited by a sol–gel method. All samples annealed in O_2 atmosphere at temperatures ranging from 650 to 750 °C showed hysteretic $C-V$ characteristics, and the memory window width in the sample annealed at 750 °C for 30 min was about 3.0 V for a voltage sweep of ±10 V. It was also found that the capacitance values biased in the hysteresis loop were unchanged over 12 h. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1380246]

Recently, studies on ferroelectric-gate field-effect transistors (FETs) have become more and more popular, because they are key components for realizing FET-type ferroelectric random access memories. However, if a ferroelectric film is directly deposited on a Si substrate, interdiffusion of constituent elements occurs as well as forming a transition layer with poor quality at the interface, and thus good electrical properties of the interface cannot be expected. In order to solve this problem, a buffer layer with a high dielectric constant is often inserted between the ferroelectric film and Si substrate forming a MFIS structure. Typical buffer layer materials are $SrTiO_3$,[1] Y_2O_3,[2] Si_3N_4,[3] and Bi_2SiO_5,[4] and relatively good interface properties have been reported in these materials. However, the data retention characteristics are not necessarily good in these MFIS devices, except for the case of Bi_2SiO_5.[4]

In order to solve this short retention time problem, it is important to increase the buffer layer capacitance and, at the same time, to decrease the leakage current.[5] In this letter, we choose $LaAlO_3$ as a buffer layer material because it has a relatively high dielectric constant (23–26),[6,7] and because the heat of the formation values of both Al_2O_5 and La_2O_3 are so large that a transition layer such as SiO_2 is expected not to be formed. $LaAlO_3$ has a nearly cubic perovskite crystal structure at room temperature with a lattice constant of 0.536 nm.[8] There are several reports on the growth of $LaAlO_3$ films on such oxide substrates as $SrTiO_3$ and CeO_2/Al_2O_3, which were deposition by the metal–organic chemical–vapor-deposition method,[9] pulsed-laser deposition method,[10] and rf magnetron sputtering method.[11] However, there is no report on the growth of a $LaAlO_3$ film on a Si substrate.

In this letter, we report on thin $LaAlO_3$ films that were formed on Si substrates using a vacuum evaporation method, and ferroelectric $Sr_{0.8}Bi_{2.2}Ta_2O_9$ (SBT) films that were deposited on the $LaAlO_3/Si$ structures using the sol–gel spin-coating method. It is shown that $LaAlO_3$ is promising as a gate dielectric in advanced metal–oxide–semiconductor FETs with a gate length shorter than 0.1 μm, as well as being useful as a buffer layer in the MFIS FET.

N-type Si(100) wafers were used as a substrate. After wet-chemical cleaning, the wafers were dipped in a diluted HF solution to remove the surface oxide and loaded into a vacuum evaporation apparatus. In order to deposit the $LaAlO_3$ film on the substrate, single-crystal pellets were heated using an electron-beam gun and the substrate temperature was kept at room temperature. The base pressure and deposition pressure in the chamber were lower than 7×10^{-7} and 5×10^{-6} Torr, respectively. The growth rate was in the range from 0.5 to 50 nm/min and the thickness of the $LaAlO_3$ films was 18–80 nm. After the deposition, a part of the wafer was annealed *ex situ* in an electric furnace at 700 °C for 10 min in N_2 ambience.

SBT films were deposited on the $LaAlO_3/Si$ structure using the sol–gel spin-coating method. The composition of the sol–gel solution was $Sr_{0.8}Bi_{2.2}Ta_2O_9$. The deposited film was dried at 150 °C for 5 min in air in order to remove organic materials and fired at 500 °C for 30 min in O_2 ambience. After repeating this process six times, the film was crystallized using an electric furnace at 650–750 °C for 30–60 min in O_2 ambience. The crystallinity of both $LaAlO_3/Si$ and $SBT/LaAlO_3/Si$ structures was analyzed by x-ray diffraction analysis. For measurements of the electrical

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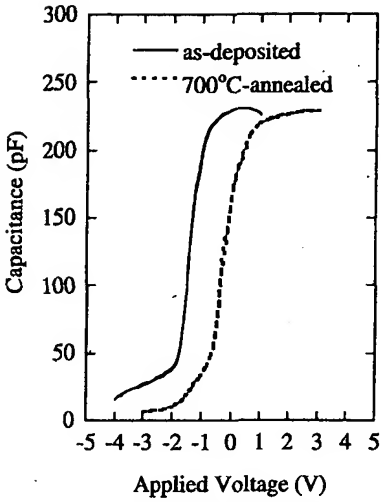

FIG. 1. $C-V$ characteristics for Al/$LaAlO_3$/Si diodes with and without postannealing.

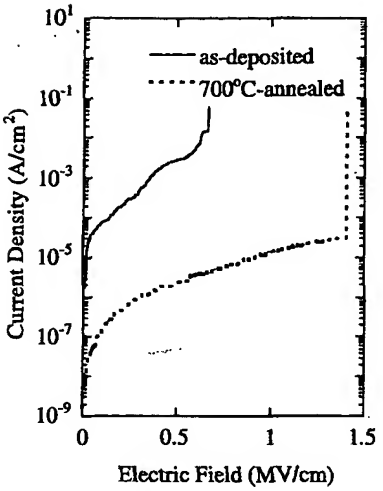

FIG. 2. Current density–electric-field ($J-E$) characteristics for the same Al/$LaAlO_3$/Si diodes as those in Fig. 1.

properties, dot-shaped upper Al and Pt electrodes were formed on $LaAlO_3$/Si and SBT/$LaAlO_3$/Si structures, respectively, at room temperature by vacuum evaporation using a metal mask. Capacitance–voltage and current–voltage characteristics were measured by an *LCR* meter and a precision semiconductor parameter analyzer, respectively.

First, we measured the crystallographical properties of the $LaAlO_3$ films by x-ray diffraction analysis. However, no diffraction peaks related to the crystal planes of the $LaAlO_3$ film were observed even in the annealed samples. Figure 1 shows typical $C-V$ characteristics for Al/$LaAlO_3$/Si(100) diodes measured at 1 MHz. The thickness of the $LaAlO_3$ film was 25 nm. The film was deposited at room temperature (solid line) and subsequently annealed at 700 °C for 10 min (broken line). Using the accumulation capacitance value of the $C-V$ curve, the relative dielectric constant of the $LaAlO_3$ film is estimated to be about 21. Since the dielectric constant increases to 24 in the sample with a film thickness of 80 nm, the lower dielectric constant in the 25-nm-thick sample may contribute to the formation of a thin transition layer at the interface between the $LaAlO_3$ film and Si substrate. The equivalent oxide thickness calculated from the accumulation capacitance is about 4.7 nm in the 25-nm-thick sample.

It can also be seen from Fig. 1 that the $C-V$ curve of the as-deposited sample is shifted in the negative direction, which is probably caused by oxygen deficiency during the $LaAlO_3$ deposition. This speculation is supported by the fact that the shift of the $C-V$ curve disappears after the annealing treatment, in which the residual oxygen gas in N_2 ambience may play an important role. It is interesting to note from the unchanged accumulation capacitance that the thickness of the transition layer, if it exists, does not increase by annealing. Since there is no hysteresis in the $C-V$ characteristics in Fig. 1, it is expected that both charge injection and ion-drift effects are negligible in the fabricated $LaAlO_3$/Si structure.

Figure 2 shows the current density versus electric-field characteristics for the same samples as those in Fig. 1. The leakage current density values at 500 kV/cm are about 2×10^{-3} and 2×10^{-6} A/cm^2 for the as-deposited and annealed samples, respectively. That is, the leakage current density was improved by about three orders of magnitude after postannealing. Figure 2 also shows that the breakdown characteristic was improved from 0.7 to 1.4 MV/cm by annealing. These are probably due to the fact that the oxygen concentration in the film reached the stoichiometric value during the annealing process.

Next, the SBT films were deposited on the $LaAlO_3$/Si structures, and their crystallographical and electrical properties were investigated. In this experiment, the thicknesses of the $LaAlO_3$ and SBT films were 25 and 210 nm, respectively. The typical x-ray diffraction patterns of the SBT films on the $LaAlO_3$/Si structure are shown in Fig. 3. As can be seen from Fig. 3, the obtained SBT films are polycrystalline and the intensity of the diffraction peaks becomes stronger at a higher temperature. Figure 3 also shows that no diffraction peaks from $LaAlO_3$ appear even after annealing at 750 °C.

Figure 4 shows the 1 MHz $C-V$ characteristic for the SBT/$LaAlO_3$/Si structures annealed at different temperatures. The samples are the same as those in Fig. 3. As can be seen from Fig. 4, both samples show counterclockwise hysteresis, as indicated by arrows, and the memory window width is wider in the sample annealed at a higher temperature. The values were 1.3, 1.7, and 3.0 V for postannealing at

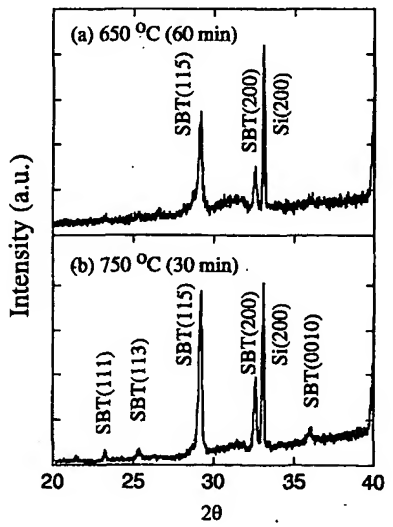

FIG. 3. Typical x-ray diffraction patterns for SBT/$LaAlO_3$/Si(100) structures crystallized at 650 °C for 60 min (a) and at 750 °C for 30 min (b).

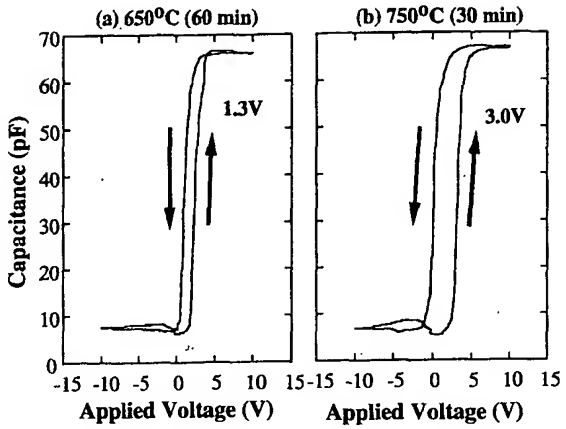

FIG. 4. $C-V$ characteristics of Pt/SBT/$LaAlO_3$/Si diodes.

650 °C for 60 min, 70 °C for 30 min, and 750 °C for 60 min, respectively. In order to check the effect of mobile ionic charges to the hysteresis loop, the scanning speed of the bias voltage was changed from 0.01 to 0.75 V/s in the $C-V$ measurement. In this measurement, the memory window width did not change within the scanning speed range investigated, which suggests that the hysteresis characteristic is due to ferroelectricity.

Finally, the retention characteristic of the above SBT/$LaAlO_3$/Si structures was investigated. Figure 5 shows the comparison of the measured retention characteristic of the SBT/$LaAlO_3$/Si structures. In this measurement, after the "write" voltage of +10 or −10 V was applied to the sample,

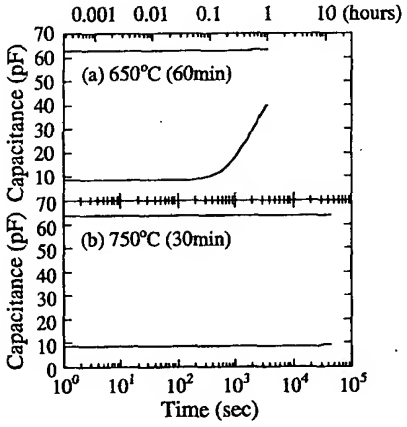

FIG. 5. Retention characteristics of Pt/SBT/$LaAlO_3$/Si diodes. The higher and lower capacitance values were measured separately, keeping the bias voltage in the middle of the hysteresis loop.

the time dependence of the capacitance was measured keeping the bias voltage at 2.0 V. As can be seen from Fig. 5, the capacitance values did not change over 12 h, when the sample were annealed at 750 °C. The result was almost the same for the sample annealed at 700 °C. On the other hand, the retention time of the SBT film annealed at 650 °C was about 1 h. The origin of the short retention time in the 650 °C-annealed sample is considered due to the insufficient ferroelectricity of the SBT film.

In summary, we formed $LaAlO_3$ thin films on a Si substrate by a vacuum evaporation method. The crystallographical property of the $LaAlO_3$ films was amorphous even after annealing at 700 °C. No hysteretic characteristic was observed in the $C-V$ curve of the MIS diodes and the dielectric constants of the $LaAlO_3$ film was estimated to be 21–24. It was also found that the electrical properties of the MIS diodes were much improved when they were annealed in N_2 ambience with some residual oxygen. Then, SBT films were deposited on the $LaAlO_3$/Si(100) structures using a sol–gel method. In these samples, hysteresis loops due to the ferroelectricity of the SBT films were observed in the $C-V$ characteristics, and the films showed excellent retention characteristics. We conclude from these results that $LaAlO_3$ is one of the most promising candidates for a high-dielectric-constant gate insulator, as well as a buffer layer for fabricating MFIS FETs.

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